A Fully Integrated 384-Element, 16-Tile, *W*-Band Phased Array With Self-Alignment and Self-Test

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***Abstract*— This paper describes the design and implementation of a scalable *W*-band phased-array system, with built-in self-alignment and self-test, based on an RFIC transceiver chipset manufactured in the TowerJazz 0.18-μm SiGe BiCMOS technology with f_T/f_{MAX} of 240/270 GHz. The RFIC integrates 24 phase-shifter elements (16TX/8RX or 8TX/16RX) as well as direct up- and down-converters, phase-locked loop with prime-ratio frequency multiplier, analog baseband, beam lookup memory, and diagnostic circuits for performance monitoring. Two organic printed circuit board (PCB) interposers with integrated antenna sub-arrays are designed and co-assembled with the RFIC chipsets to produce a scalable phased-array tile. Tiles are phase-aligned to one another through a daisy-chained local oscillator (LO) synchronization signal. Statistical analysis of the effects of LO misalignment between tiles on beam patterns is presented. Sixteen tiles are combined onto a carrier PCB to create a 384-element (256TX/128RX) phased-array system. A maximum saturated effective isotropic radiated power (EIRP) of 60 dBm (1 kW) is measured at boresight for the 256 transmit elements. Wireless links operating at 90.7 GHz using a 16-QAM constellation at a reduced EIRP of 52 dBm produced data rates beyond 10 Gb/s for an equivalent link distance in excess of 250 m.**

***Index Terms*— 5G, 90 GHz, beamforming, coherent beam, flip-chip, fully integrated, gigabit wireless link, high effective isotropic radiated power (EIRP), integrated antenna, large-scale array, MIMO, millimeter-wave (mm-wave), multi-beam, phase shifter, phase-locked loop (PLL), phased array, self-aligned, self-test, tile, vector modulator, *W*-band.**

I. Introduction

ADVANCED SiGe BiCMOS, CMOS, and InP HBT processes continue to push the frontier on millimeter-wave (mm-wave) and highly integrated phased-array systems for a variety of communication, radar, and imaging applications [1]–[11]. Furthermore, next-generation mobile technology (5G) demands ultra-low latency and high data rates with ubiquitous deployment supporting multiple users through the use of picocells [12]. These cells may require up to hundreds of active elements capable of forming multi-gigabit per second wireless links at distances greater than hundreds of meters and producing thousands of highly directive beam patterns [13]. To make the wide adoption of such mm-wave systems a reality, the overall cost of the system must be significantly reduced. This can be accomplished through several means. First, producing highly integrated phased arrays eliminates the need for additional external components (such as expensive mm-wave synthesizers, amplifiers, and switches), which reduces the overall system costs. Second, eliminating exotic packaging processes and materials would allow for low-cost traditional manufacturing techniques to be applied to mm-wave systems. Third, incorporating self-test, fault detection, health monitoring, and self-calibration into the RFIC significantly reduces the costs of factory testing (by eliminating the need for any mm-wave verifications) and enables remote maintenance and system reconfiguration in case of failures. Finally, architecting a scalable phased-array tile as a building block for larger mm-wave arrays provides flexibility in system design based on specific link budget requirements. In general, phased-array system architecture is heavily influenced by path losses and transmission line (TL) losses. Hence, there have been several demonstrations with varying levels of integration depending on the frequency range, as shown in Fig. 1.

Fig. 1. Collection of demonstrated mm-wave RFIC phased-array systems that explore various frequency ranges, integration levels, and tiling methods.

At 28 and 39 GHz, there are two distinct approaches to phased-array architecture: 1) distribution at RF, where 4- to 8-element TRX RFIC phased arrays with phase shift and gain control are combined together through passive networks to a single I/O port on a common substrate, and the up/down conversion to an IF or baseband is performed off chip [14]–[16] and 2) distribution at a lower frequency local oscillator (LO) and IF, where 16- to 32-element TRX RFIC phased arrays are

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further integrated with up-/down-conversion and phase-locked loop (PLL) circuits and can be combined on a common substrate or at a modular level [1], [3], [14], [17]. A summary of the tradeoffs between these different architectures at 28 GHz can be found in [1]. At 60 GHz, approaches to integrated and/or scalable phased arrays based on power-combining at IF and LO [5] and RF [4], [9], [18]–[20] have also been demonstrated. At *W*-band frequencies (75–110 GHz), however, RF distribution becomes increasingly difficult to implement on conventional substrate materials due to higher insertion losses [6]. Since a tiled approach is required for creating arrays with hundreds of active elements, the frequency of operation will force a balance between RF and IF distributions. This overall frequency-dependent system architecture can be observed in the examples provided in Fig. 1 where higher mm-wave frequency phased-array ICs are (often) more tightly integrated.

The *W*-band is of particular interest for longer range communication systems due to the local minimum in atmospheric absorption near its center [6], [21], [22] as well as the ample available bandwidth. In February 2018, the Federal Communications Commission (FCC) proposed an adoption of rules for fixed point-to-point (PTP) use of multi-gigahertz spectrum in various bands above 95 GHz, including four bands between 95 and 109.5 GHz. Moreover, the FCC noted that there has been a recent increase in interest in these bands and that there has been an urgent market demand for 50–400 Gb/s wireless backhaul for 5G systems [23]. In this paper, we present the third-generation implementation of a highly integrated and scalable phased-array chipset for steerable-beam and spectrally efficient wireless data links at *W*-band [24], [25]. The overall system includes a 384-element, 16-tile phased array with built-in self-alignment and self-test and addresses mm-wave PTP and point-to-multipoint (PTMP) applications.

This paper is organized as follows. Section II presents the phased-array chipset architecture and circuit design with the detailed block diagrams and schematics of critical components. Also, the LO daisy-chaining architecture is demonstrated and the effects of multi-tile LO phase alignment impairments are discussed. Section III presents the design, implementation, model, and simulation of the tile with integrated antenna array. Additionally, antenna element locations are discussed in relation to a larger scalable phased array that is required for proper self-alignment and self-test. Section IV demonstrates a multi-tile hardware platform, including mechanical design and thermal analysis. Section V presents individual chipset and multi-tile measurements, phased-array antenna beam patterns, and wireless link performance and limitations. Conclusion are given in Section VI.

II. Chipset Architecture

The new generation of phased-array modules presented in this paper addresses the challenges for large-scale integration, scalability, and multi-tile synchronization. Bidirectional TRX elements require switches to isolate the low noise amplifier (LNA) and PA during the time division duplex (TDD) operation. The loss and linearity impact of such a switch network, implemented in a 0.18-μm SiGe BiCMOS and operating at

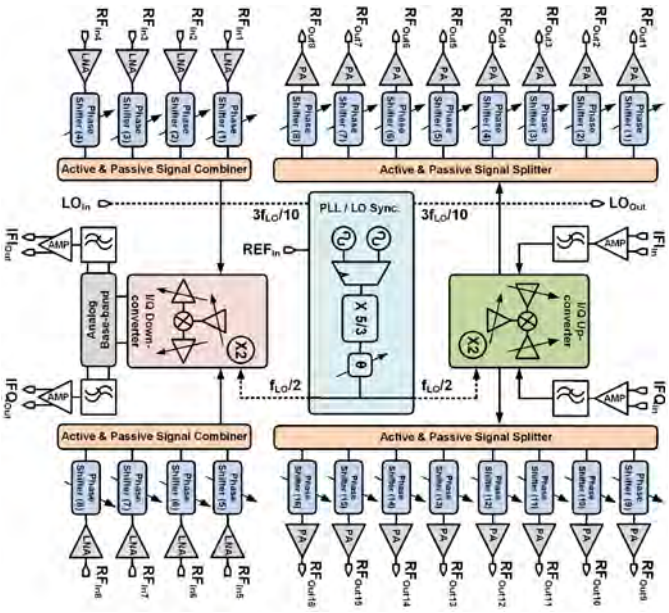

Fig. 2. Simplified block diagrams of the 16TX/8RX *W*-band phased-array RFIC. An 8TX/16RX version of the RFIC is also implemented. The large-scale phased-array system is comprised of the 16 identical chipsets.

W-band, has been deemed excessive, and therefore, separate TX and RX phased-array elements are implemented. Each *W*-band phased-array IC comprises a full transceiver architecture with either 16TX/8RX or 16RX/8TX calibrated active elements (see Fig. 2). The two implemented variants of the IC provide flexibility of deployment in scenarios where a larger receiver aperture may be desirable or where bidirectional communication requires an asymmetric link budget, such as different up- and down-link data rates.

Each chip is also equipped with direct up- and down-converter mixers as well as a fully integrated PLL with a prime-ratio mm-wave multiplier in order to avoid voltage controlled oscillator (VCO) pulling. A high dynamic-range analog baseband block with programmable filter bandwidth is also included. Passive and active signal distributions provide the RF signal path to all phase-shifter elements, and a distributed digital Serial Peripheral Interface (SPI) is used for calibration, self-test, and health monitoring. Each chipset includes more than 175 internal monitor and diagnostic points with 29 on-chip ADCs for digital readouts as well as a 32-slot beam lookup table for rapid beam hopping.

1) Transmit and Receive Phase-Shifter Architectures: The simplified block diagram of the transmit and receive phase-shifter elements is shown in Fig. 3. The 5-bit active phase shifting is accomplished through vector summation, and the performance has been demonstrated in the previous generation RFICs in [8] and [25]. In this chipset, each receive element additionally employs a built-in coupler, amplifier, and variable gain amplifier (VGA) chain followed by a power detector in order to independently monitor the performance of the element during self-test procedures. To keep the overall RFIC dimensions minimized, the additional diagnostic blocks incorporated into each element should not contribute significantly to the occupied area. Consequently, the RF monitor

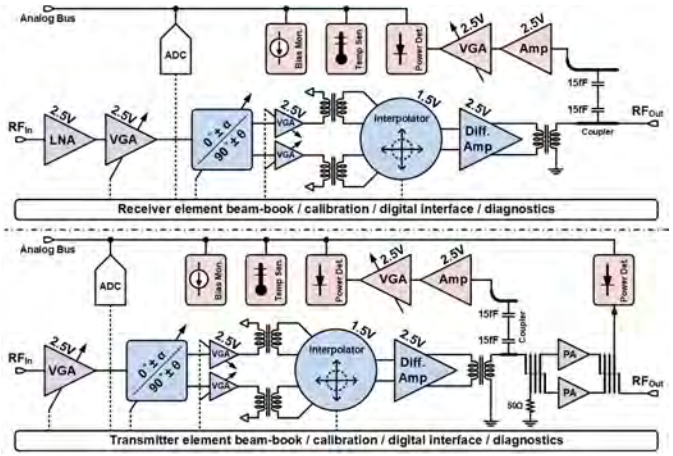

Fig. 3. Simplified block diagrams of the receiver (top) and transmitter (bottom) phase-shifter elements based on a vector modulator architecture. Each element is equipped with diagnostics and health-monitoring circuitry.

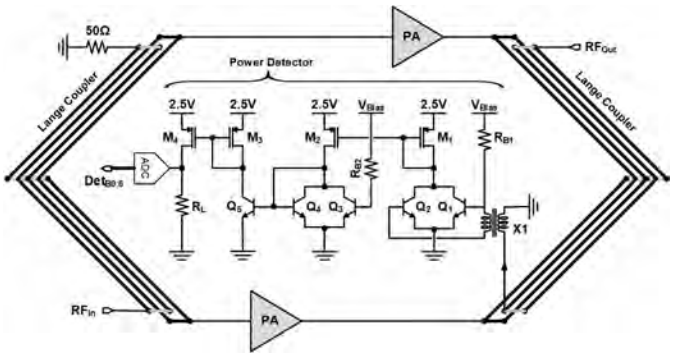

Fig. 4. Architecture of the implemented balanced PA that employs a pair of Lange couplers and a power detector at the isolation port for antenna and PA failure detection.

path uses capacitive couplers with less than 10-μm^2 footprint. Two minimum-size capacitors of 15 fF in series provide a 20-dB coupler at 90 GHz. The impact of the coupler on the main RF path is negligible (below 0.2dB). The transmitter element uses an extra power detector on the isolation port of the balanced power amplifier (PA). The isolation port behaves as a reflectometer and can be used to detect antenna failures or strong reflected signals. The VGA on the RF diagnostic path is designed to counter the VGA on the main RF path in order to provide a constant signal to the power detectors. It is important to note that the purpose of the diagnostic power detectors is not to measure TX/RX power in an absolute sense, but rather in relative terms. During diagnostics, each RF element power is measured and compared to ensure uniformity and functionality of various phase-shifter blocks.

The maximum gain in the diagnostic path, including the coupler is 0 dB and the power detector sensitivity, is approximately -25 dBm. Therefore, the transmitter diagnostic circuitry can be used to null the LO signal at the antenna port of each element to below -25 dBm. LO nulling is accomplished by applying a dc offset at the transmit IF ports using a pair of integrated 8-bit DACs. This procedure is executed during system start-up through the SPI. Furthermore, LO rejection may be performed by the Modem/DSP at the MAC layer of the communication system once a link has been established between two phased-array radios. The transmit and receive power detectors are also used to monitor RF power uniformity, variation, and stability across all phased-array elements. Both the RF and diagnostic VGAs use a current-steered Cascode architecture, as detailed in [8]. Furthermore, the diagnostics circuitry is only enabled during self-test, fault detection, and calibration to reduce the overall system power consumption.

In addition to RF diagnostics, every element is also equipped with temperature sensors on critical blocks, such as the LNA and PA. The balanced PA architecture is shown in Fig. 4, which includes a pair of Lange couplers at the input and output of two class-A Cascode PA blocks. The isolation port of the output Lange coupler is terminated into a 50-Ω matched power detector whose schematic is also shown in Fig. 4. All integrated diagnostic ADCs are implemented as 8-bit successive-approximation converters, which can be accessed through the SPI. Furthermore, bias monitor blocks and local digital-loopback paths are used to verify the correct operation of both analog and digital blocks in each phase shifter. All diagnostics' information (including power supply, bias point, temperature monitor, and power detectors) is digitized locally in each element as well as routed on a global analog bus. This global bus is also routed to an IC pin to allow the use of an external ADC with higher resolution and accuracy. The circuitry responsible for diagnostic functions is disabled during normal operation and therefore do not consume additional power. The ADC and digital blocks do not consume any static power and their dynamic power consumption ($<$0.5 mW) is insignificant relative to the RF blocks.

All active elements are equipped with calibration memory and beam lookup tables. During system start-up or operation, up to 32 unique beam patterns can be loaded into every element's local memory, which enables rapid beam hopping. This beam lookup table allows the entire 16-tile phased-array system to be simultaneously steered to a desired direction through a single digital broadcast command. At an SPI rate of 50 MHz and 16-bit addressing, issuing a new beam direction requires only 320 ns for 16 tiles (384 active elements). It is important to note that SPI commands can also be issued during live traffic, while the array is in operation. Therefore, the beam-hop command duration only determines the shortest possible packet size between beam hops and not the dead zone, while the beam is being steered by the phase shifters. Furthermore, to minimize any dead-zone duration, a dedicated beam latch and transmit/receive digital IOs are also implemented to allow TDD switching without issuing SPI commands. The measured beam steering and transmit/receive switching speeds are presented in Section V.

A. Up- and Down-Converter Architectures

The RF signal routing, to and from each phase shifter, is accomplished through a combination of active and passive signal distribution [8]. In order to balance tradeoffs

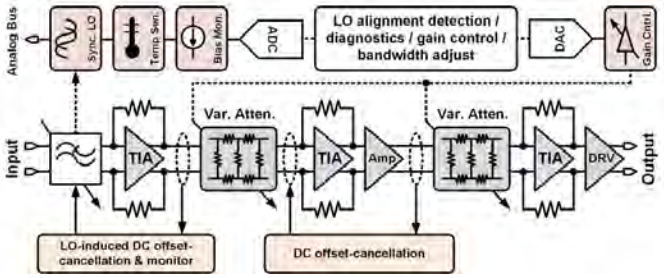

Fig. 5. Simplified block diagram of the I/Q analog baseband VGA with 42 dB of gain control and up to 3 GHz of adjustable bandwidth.

between linearity, signal attenuation, and added RF noise, only a single active power combiner/splitter is used in the RF signal distribution network. The remaining RF distribution is handled through harmonic-rejecting Wilkinson power dividers and combiners [8]. All frequency translations use direct-conversion (zero IF) architectures. The transmitter employs 4-bit, IF VGAs with ±3 dB of range, which can be used for I/Q amplitude imbalance correction. Furthermore, the VGAs incorporate a first-order *RC* filter to attenuate unwanted and out-of-band spurious tones before the up-conversion mixer. The IF VGAs also incorporate 8-bit DACs to enable up to ±100 mV of dc offset at the input of the up-conversion mixers to minimize transmitter LO leakage. The RF diagnostic tools incorporated into each phase shifter can be used to detect and aid in the cancellation of LO feedthrough, as described in Section V.

In this chipset, in addition to the blocks described in [8], [24], and [25], the receiver also employs an RF VGA before the down-conversion mixer, which, in conjunction with the RF VGA in the phase shifters, provides an extra degree of freedom to trade off overall receiver gain, noise, and linearity performance. A full I/Q analog baseband chain is added after the down-conversion as described in Section II-A1.

1) I/Q Analog Baseband Architecture: The analog baseband block performs two important functions. It is responsible for providing variable IF gain as well as canceling any LO-induced dc offsets originating from the I/Q down-convert mixers. Traditionally, the dc cancellation circuitry serves no other purpose than ensuring the high-gain IF amplifier stages that are not saturated under strong LO injection conditions. In this design, however, the detected I/Q dc terms are internally digitized and used in a novel calibration scheme to measure the relative phase between tiles in the multi-tile phased-array system.

The block diagram of the baseband chain is shown in Fig. 5. It consists of a tunable low-pass active filter providing filtering for I/Q IF channel bandwidths from 0.7 to 3 GHz in 16 different steps. This corresponds to RF channel bandwidths between 1.4 and 6 GHz. The active filter is implemented using a multiple feedback (MFB) filter topology by realizing a third-order Chebyshev low-pass filter around a trans-impedance amplifier (TIA), which acts as the load for the RF mixer in the receiver (see Fig. 6). Care has been taken to ensure that the TIA input impedance remains constant at about 50 Ω within the filter

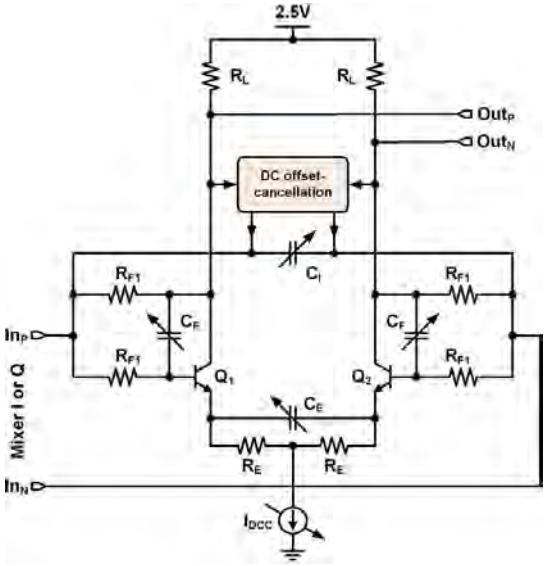

Fig. 6. Schematic of the front-end TIA amplifier and dc offset cancellation block that interface to the I/Q mixers.

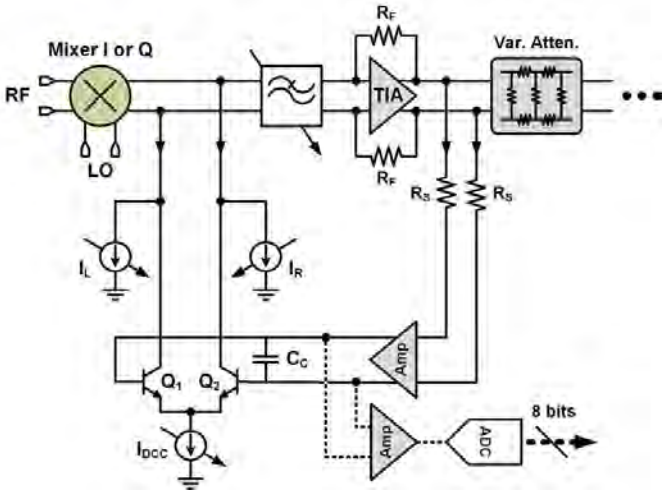

Fig. 7. Schematic of the offset cancellation block responsible for LO-induced dc cancellation and monitoring. The digitized I/Q dc signals are used for tile-to-tile alignment procedure.

bandwidth across all filter settings. All variable capacitors are implemented using a combination of digital varactors and MOS-switched metal–insulator–metal (MIM) capacitors. DC cancellation is achieved by two continuous feedback loops at the input of both the baseband chain and the first VGA. The first dc cancellation circuit injects correction currents at the interface between the down-conversion mixer and the TIA input in order to counteract the LO-induced dc offset (see Fig. 7). The digitally adjustable current sources I_L and I_R can be set through the SPI and may be used to cancel dc offsets due to component mismatches or to purposely introduce a dc offset to verify the correct behavior of the feedback loop and internal ADC. The analog feedback loop performs the dynamic dc offset cancellation continuously without invoking the SPI, which is reserved for beam switching during live traffic and TDD modes. The capacitor C_C is part of the

low-pass filter of the dc cancellation feedback network. The range of dc cancellation is tunable in order to keep added noise to a minimum. LO-induced dc offsets of up to ±2 mA at the mixer outputs can be canceled. Time-invariant dc offsets due to mismatches can be corrected by switchable current sinks implemented at the output of the mixer [IL and infrared (IR)]. This is beneficial since it enables the dc offset cancellation circuit to always operate at the optimum bias settings.

The analog filter is followed by two interpolated-ladder-attenuator VGAs with a total gain of 42 dB. The gain of the VGAs can be controlled independently either by an analog control or digitally through the SPI using an internal 8-bit DAC. The final stage of the baseband chain is a linear output driver with 50-Ω on-chip terminations to drive the 100-Ω differential input of an external ADC. The baseband chain provides sufficient bandwidth to support data rates beyond 10 Gb/s as well as sufficient linearity to process spectrally efficient modulation, such as 256-QAM. The complete I/Q baseband consumes 250 mW from dual 2.5-/1.5-V supplies. All IF ports are externally ac coupled due to the modem requirements. The internal residual dc offsets are less than a few millivolts.

B. Phase-Locked Loop and LO Architecture

A major challenge in the design of large-scale multi-die phased-array systems operating at mm waves is the LO distribution and chip-to-chip synchronization. Furthermore, due to the large radiated power in systems employing hundreds of active transmitter elements, integrated PLLs are strongly susceptible to VCO pulling/pushing and LO signal pollution [26]. Additionally, routing mm-wave LO signals to multiple RFICs from a single source becomes increasingly impractical for systems using tens of phased-array modules (tiles). The global LO architecture of the presented large-scale phased-array system performs several key functions, including frequency translation and LO phase control for multi-tile synchronization. In this system, tile-to-tile phase alignment is accomplished by the means of a daisy-chained LO synchronization signal (see Fig. 8). Since all phased-array tiles are identical, every chipset includes all blocks necessary to accommodate both LO generation, frequency multiplication, and phase shifting. This implies that the internal PLL must operate in two modes depending on the tile location in the overall daisy-chained architecture (see Fig. 9).

In the first mode (referred to as master mode), the built-in dual VCOs are locked to a reference (nominal 1.6875 GHz) at 1/16th of the VCO frequency (nominal 27 GHz) using a second-order loop architecture. A 100-MHz crystal oscillator in conjunction with an external PLL chipset produces the 1.6875-GHz (or 1.7 GHz to operate the external PLL in the integer mode) reference frequency required for the internal PLL. Depending on the reference frequency used, the achievable carrier frequency range is between 81.5 and 97.5 GHz. The VCO fundamental frequency is chosen to be at a non-integer multiple of the carrier frequency $f_{\mathrm{VCO}} = (3 \times f_{\mathrm{Carrier}})/10$. This ensures that no mixing terms of the RF carrier and VCO frequency fall into the PLL loop bandwidth

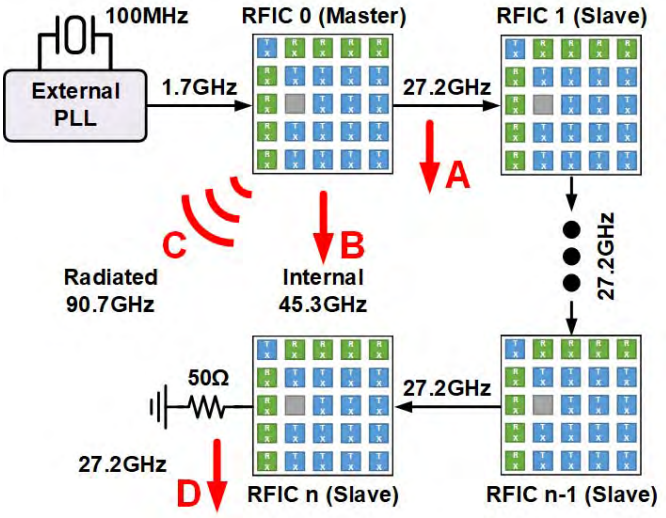

Fig. 8. Progression of the LO synchronization signal in the daisy-chained tile architecture. Phase noise measurement is performed at the indicated A, B, C, and D points.

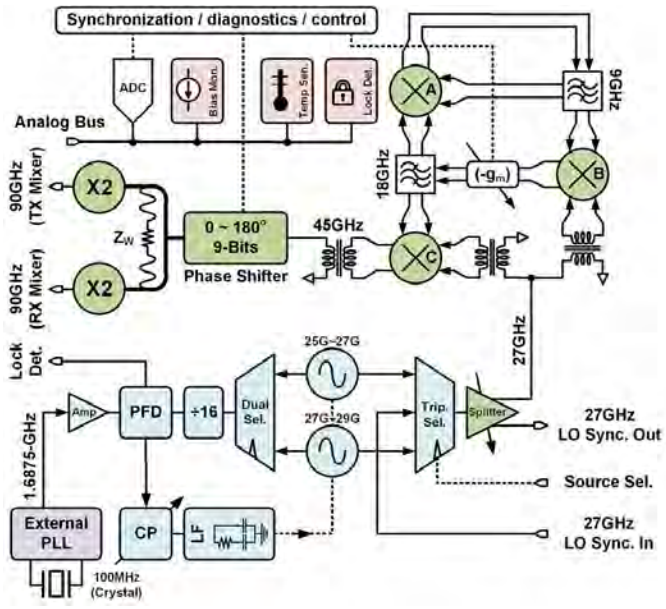

Fig. 9. Simplified block diagram of the PLL and integrated LO architecture. The PLL operates in either master or slave mode depending on the position of the chipset within the tiling structure of the full phased-array system.

(adjustable between 5 and 30 MHz) or within several gigahertz of the VCO frequency. The integrated diagnostics and self-test features of the PLL monitor critical bias conditions, such as the charge-pump output common-mode level, temperature of the VCO cores, and locked/un-locked conditions. All diagnostics data are digitized locally and are accessible through the SPI. Furthermore, critical malfunction flags, such as loss of lock, can be used to disable the PA outputs independent of SPI traffic.

The locked VCO output (nominal 27 GHz) is forwarded to the next tile as the LO synchronization signal while simultaneously further multiplied by a prime ratio of 5/3 multi-

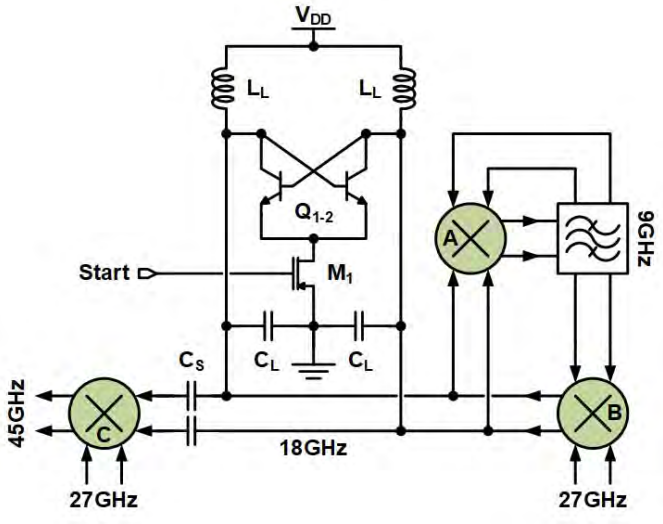

Fig. 10. Schematic of the filter and negative resistance ($-g_m$) elements at the interface of the triple-mixer frequency multiplier block.

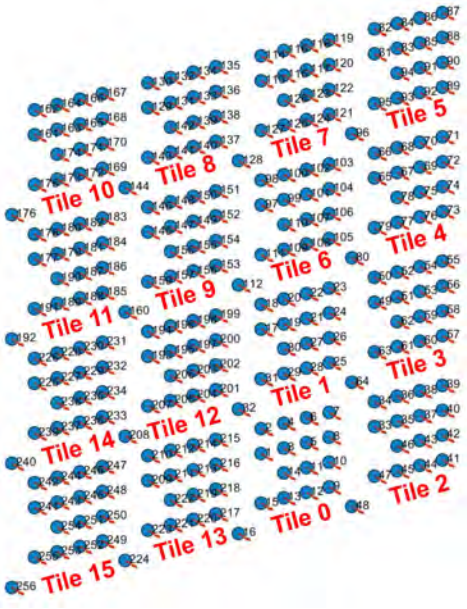

Fig. 11. Simulation model for the presented large-scale phased array comprising 16 tiles. This model includes only the 256 transmit elements where all receive elements are omitted.

plier using the shown triple-mixer architecture producing an $f_{\text{Carrier}}/2$ signal (see Fig. 9). In the second mode (referred to as slave mode), the VCO and PLL cores are shut down and the external LO synchronization signal is selected using the triple-selector block instead. The proceeding multiplication and LO forwarding blocks are active in both master and slave modes. The triple-mixer multiplier achieves the 5/3 multiplication ratio through a series of self-mixing, dividing and bandpass filtering. Mixer "A" is configured as a Miller divider whose output is tuned at 9 GHz and therefore can divide an input signal of 18 GHz by a factor of 2. Mixer "B" uses the output of the Miller divider in conjunction with the input LO synchronization signal (at 27 GHz) to produce an output signal of 18 GHz that in turn is used as the input of the Miller divider. This creates a circular relationship between the mixers "A" and "B" and provides a divide-by-3 (9 GHz) and multiply-by-2/3 (18 GHz) outputs simultaneously. It is important to note that all other undesired harmonics and mixing products are suppressed using bandpass LC networks at the input and output of each mixer as well as fully differential architecture for low fundamental leakage. In the final stage, mixer "C" multiplies the LO synchronization signal and the available mixer "B" output (at 18 GHz) to produce a 45-GHz output tone for a total multiplication ratio of 5/3. In a similar fashion, all other undesired harmonics are filtered using tuned input/output transformers.

Due to the circular input/output dependence of mixers "A" and "B," it is required that the Miller divider is presented with an input signal to start division and generate the desired divide-by-3 (9 GHz) signal. This is accomplished by using a negative resistance ($-g_m$) block comprised of cross-coupled HBT devices (Q_{1-2}) at the output of Mixer "B," as shown in Fig. 10. In combination with the tuned LC network on the same node (L_L and C_L), an oscillation frequency near the desired 18-GHz range is generated, which kick-starts the Miller divider into operation. With the PLL locked, the oscillation is injection-locked by the LO synchronization signal and all signals at the input and output of Mixers "A" and "B" become self-sustained. This start-up procedure is only applied during system power-on after which the negative resistance block is disabled. Furthermore, since the start-up phase of the Miller divider mixer cannot be predicted *a priori*, each tile will exhibit a 120° phase uncertainty after the power-on procedure [27]. Therefore, a tile-to-tile alignment algorithm must be executed before a correct beam pattern can be observed from the full system. This procedure is described in Section V.

A 180° 9-bit phase shifter is included in the path of the 45-GHz signal to allow for multi-chip LO phase alignment. The phase shifter comprises two 90° phase shifters in succession, each using a transformer-based hybrid and vector modulator architecture. The phase-shifted signal is split using a harmonic-rejecting Wilkinson power divider [8] into two equal-power paths. The final LO generation stage uses two doublers to generate the final LO signal (f_{Carrier}) required by the direct-conversion transmit and receive mixers.

C. Analyses of Multi-Tile Phase Alignment Impairments

It has been shown that multi-channel phased-array chipsets offer excellent element-to-element phase and amplitude matching within the integrated circuit [1], [4], [14]. Furthermore, the impact of individual element-to-element mismatches on beam pattern characteristics has been well studied [14]. However, considering the advantages and popularity of multi-chip large-scale phased arrays, the impact of tile-to-tile LO phase alignment must be considered.

A simulation model for the presented large-scale phased array comprising 16 tiles is used to study the impact of tile-to-tile phase alignment. This model includes only the

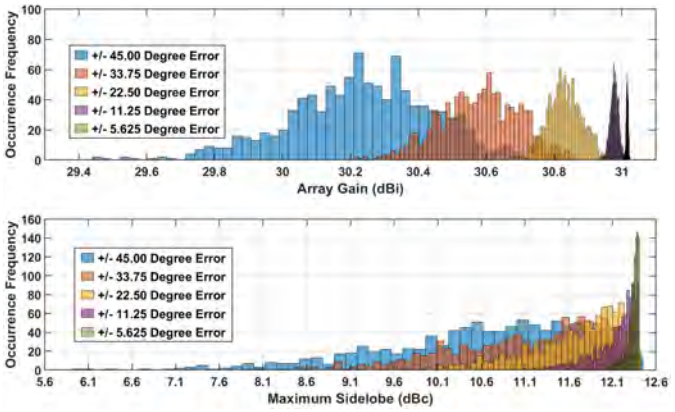

Fig. 12. Histogram of Monte Carlo simulations for both the peak array directivity (top) and the maximum sidelobe (bottom) for various tile-to-tile phase alignment errors.

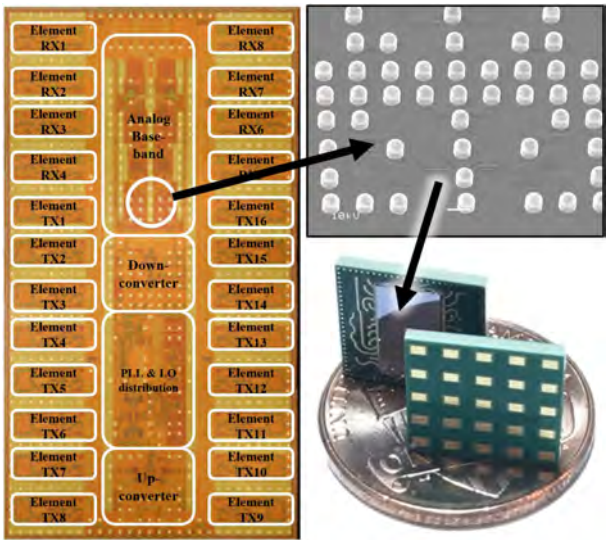

Fig. 13. Die photograph of the 24-element phased-array chipset, bumping procedure, and tile assembly.

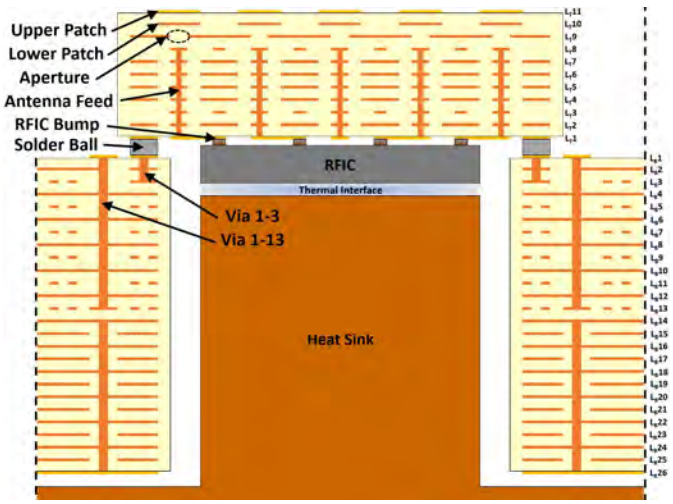

Fig. 14. Cross section of assembled tile and carrier organic PCB stack-up.

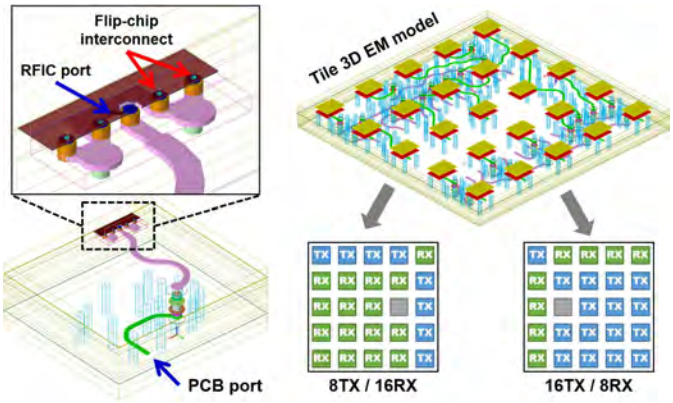

Fig. 15. Left: 3-D electromagnetic (EM) model of RFIC pad to antenna port transition. Right: 3-D EM model of 24-port 5×5 ASP antenna array.

256 transmit elements where the 128 receive elements as well as the 16 dummy elements have been omitted (see Fig. 11). In order to study the impact of tile-to-tile phase alignment error in isolation, the model assumes that within each tile, all the elements have ideal phase and amplitude matching. A set of Monte Carlo simulations are performed on the 16-tile system where intentional tile-to-tile phase errors have been introduced. The phase error is chosen randomly using a uniform probability distribution bounded within $\pm\phi$ degrees for each tile. A total of 1024 simulations are performed for each of the five distinct values of $\phi = [5.625, 11.25, 22.50, 33.75, 45.00]$ degrees. Fig. 12 shows the simulated histogram of both the peak array directivity as well as the maximum sidelobe for each distribution of phase error ϕ. It can be observed that even for tile-to-tile phase errors up to $\pm 22.5°$, the array directivity variation and the sidelobe suppression are bounded to be below 0.5 and 2 dB of their nominal values, respectively. This result is to be expected since the phase difference between the tiles only affects clusters of 16 elements at a time and therefore has a weaker impact of disturbing the beam compared with individual element-to-element mismatches. Therefore, the system alignment procedure must accomplish an average tile-to-tile phase alignment of better then $\pm 22.5°$ in order to produce consistent beam patterns.

III. Phased-Array Tile Design

The tile acts as the integrated building block for the scalable phased-array system. Each tile is comprised of an organic ball-grid-array (BGA) printed circuit board (PCB) interposer and a flip-chip RFIC, as shown in Fig. 13. The interposer is shown as the multi-layer stack-up (LT1–LT11) in Fig. 14 and its construction is compatible with conventional solder reflow processes. Two unique interposers were designed to accommodate the two RFIC chipsets, as shown in Fig. 15. The interposers provide various connections, such as SPI, analog control, baseband I/Q, LO synchronization, power, and ground signals with the main carrier PCB. Furthermore, they integrate the feed network and antenna sub-arrays for both transmit and receive phase-shifter elements as well as proper positioning of antenna elements such that their intra-tile (within a tile) and inter-tile (tile-to-tile) spacings are equivalent. Finally, the position of various antennas is chosen to enable

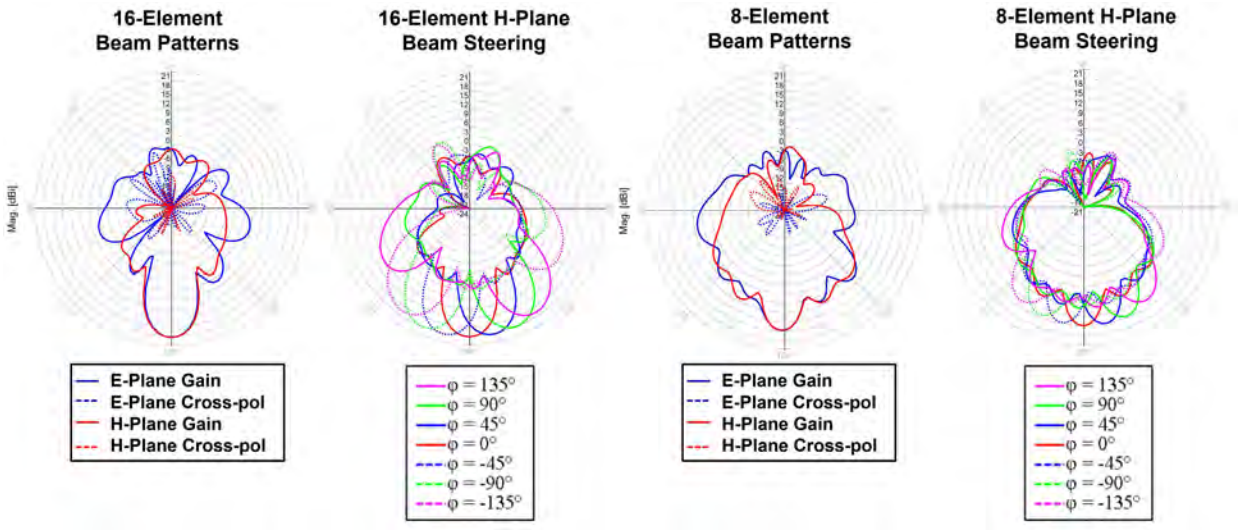

Fig. 16. Simulated (from left to right) E- and H-plane co- and cross-polarization for 16-element ASP antenna sub-array, H-plane co-polarization beam patterns, E- and H-plane co- and cross-polarization for eight-element ASP antenna sub-array, and H-plane co-polarization beam patterns.

tile-to-tile calibration through the adjacent transmit and receive elements.

A. RFIC Fan-Out and Interconnect

Each RFIC chipset is flip-chip attached to layer LT1 (see Fig. 14) of the interposer. Layers LT1 and LT3 were used to route all SPI, analog control, baseband, and LO synchronization signals, and layers LT5 and LT6 were used for power distribution. Keysight ADS was used to design and simulate the EM performance of the LO synchronization, I/Q paths, and its multi-layer transitions to the carrier PCB [28]. Keysight PIPro was used to optimize the dc IR drop for each power plane contained within the interposer [29].

B. RF Feed Network and Antenna Array Integration

RF port flip-chip transitions to and from the interposer LT1 pads were designed and simulated using Keysight ADS and EMPro [28], [30]. Fig. 15 shows the 3-D EM model of the complete transition from the RFIC pad to the antenna port. The antenna feeds are comprised of microstrip TLs and coaxial vias spanning layers LT1–LT8 and are broadband matched to 50 Ω from dc to 110 GHz to provide a low-loss pathway between each RF port and antenna element [31], [32]. Careful simulation and co-optimization of the input and output return loss of the RFIC PA and LNA with and without the complete antenna feed lines are performed. Due to layout restrictions and space constraints, all antenna feeds are not equal in length and, instead, are phase-matched to 180° steps at 90 GHz.

The integrated 5 × 5 antenna array is partitioned into 16-element and 8-element aperture-stacked patch (ASP) antenna sub-arrays to interface with the 24 phase-shifter elements. This ASP antenna architecture provides medium gain and large bandwidth and can be constructed using the standard PCB processes [33]. The resonant aperture is designed into layer LT8, and the lower and upper patches of each antenna element are designed into layers LT10 and LT11 (see Fig. 14). Layer LT2 is utilized as an antenna reflector to minimize any back radiation and to better shield the RFIC. The antenna elements are spaced at 0.63λ (2.1 mm) at 90 GHz in both the E-plane and the H-plane. Ideally, the elements would be spaced at 0.5λ; however, due to physical constraints set by the RFIC as well as PCB process limitations, such a scheme was not possible. The increased antenna spacing contributes to additional grating lobes observed in the overall beam patterns. Fig. 15 shows the 3-D EM model of the 24-port 5 × 5 ASP antenna array with simulated directivity, gain, and efficiency of better than 18 dB, 18.5 dB, and 87%, respectively. The simulated return losses of the 16- and 8-element ASP antenna sub-arrays are approximately −10 dB from 80 to 100 GHz. Although this system operates in the TDD mode where TX and RX elements never operate simultaneously, it is important to minimize mutual coupling between TX and RX antennas to reduce any observed impedance variations at the PA/LNA ports. The simulated mutual coupling from a sample transmit port to each of the other eight receive ports is also better than −20 dB between 80 and 100 GHz. Fig. 16 shows the simulated E- and H-plane co- and cross-polarization beam patterns as well as H-plane beam steering patterns for both the 16- and 8-element antenna sub-arrays. The eight-element beam pattern exhibits higher grating lobes due to the sparse placement of the RX elements. However, in situations where a symmetric RX beam pattern is required, the 8TX/16RX antenna configuration may be used.

C. Antenna Element Positioning

The exact partitioning of the 24 antenna elements in each of the two interposers can be seen in Fig. 15. The location of the transmit and receive antenna elements is chosen to achieve 2-D beam steering for any number of tiles. Furthermore, the antenna element arrangement provides bidirectional element-to-element coupling paths between the adjacent tiles on any of the four edges which is used for the tile-to-tile alignment procedure.

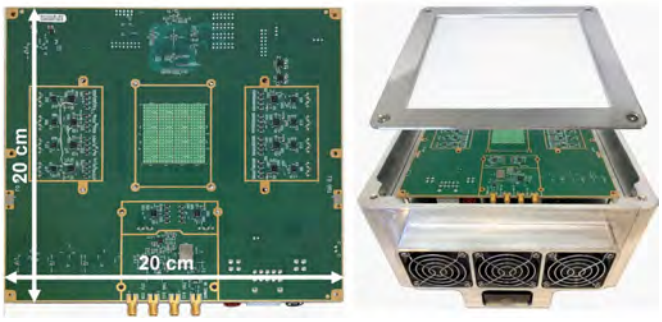

Fig. 17. Assembled 16-tile carrier PCB (left) and radio-head enclosure for the assembled 384-element, 16-tile phased-array system (right).

IV. Carrier PCB Design

The carrier PCB was designed to accommodate up to 16 tiles and is shown as the multi-layer stack-up (LB1–LB26) in Fig. 14. It was constructed using the same organic material as the interposers to minimize CTE mismatches during assembly and operation. Tile-to-tile LO daisy-chaining on the carrier PCB is realized through microstrip and stripline TLs on layers LB1 and LB3, respectively, and are interconnected vertically through Vias 1–3. Layers LB1–LB13 and Vias 1–13 were used to fan out all input and output baseband I/Q signals, which are routed differentially to reduce coupling to/from other signals. Keysight SIPro is used to phase match and validate the signal integrity of all baseband routes [29]. Fig. 17 shows an assembled carrier PCB populated with 16 tiles. The carrier PCB includes an external PLL with integrated VCO and a 100-MHz VCXO to generate a tunable reference for the RFIC PLL (see Fig. 9). A 50-Ω resistive splitter and a combiner network are added to distribute baseband I/Q signals, and differential switches are used to direct the I/Q to either all 16 tiles or four quadrants of 4 tiles (see Fig. 18). Moreover, a hole is routed in the carrier PCB at each tile location to allow for a heat sink to make a direct contact with each of the RFICs.

The thermal performance of the heat-sink solution is analyzed in COMSOL Multiphysics and its temperature gradient is plotted in Fig. 19. This worst case scenario assumes that each RFIC is operating at maximum power where all transmit and receive elements of the RFIC are active as well as all RF diagnostic components. The resulting temperature observed is approximately 53.5 °C at an ambient temperature of 23 °C. The thermal image includes the impact of the dc/dc converter modules located at the corner of the PCB. It is important to note that during normal wireless link operation, the RFIC diagnostic elements are disabled and the system operates in the TDD mode. The complete 16-tile carrier PCB assembly with heat sink and radio-head enclosure is shown in Fig. 17. The unit is mountable on light poles, buildings, and cell towers.

V. Fabrication and System Measurements

The phased-array chipset is implemented in the TowerJazz 0.18-μm SiGe BiCMOS process with f_T/f_{MAX} of 240/270 GHz. The process offers 0.18-μm CMOS transistors and seven layers of aluminum metallization. Each IC

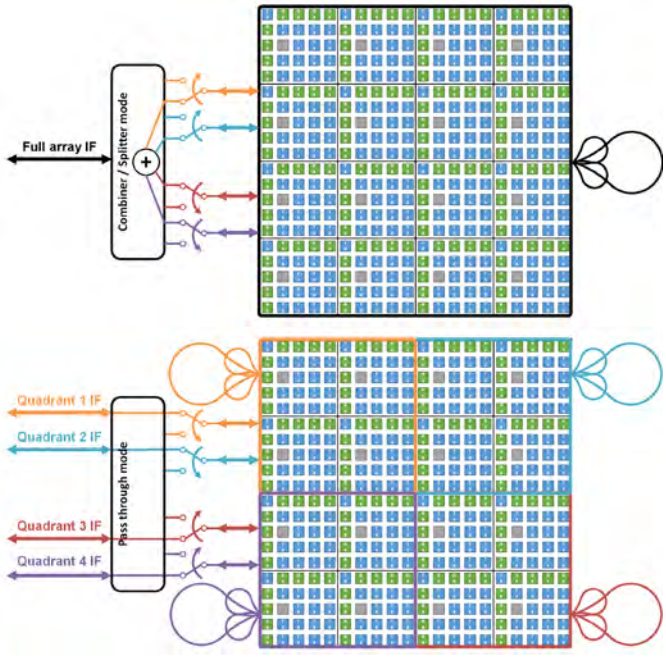

Fig. 18. Top: 384-element, 16-tile phased array configured as fully cohered system. Bottom: 384-element phased array sub-divided into four quadrants of 4 tiles in order to generate four independent beams.

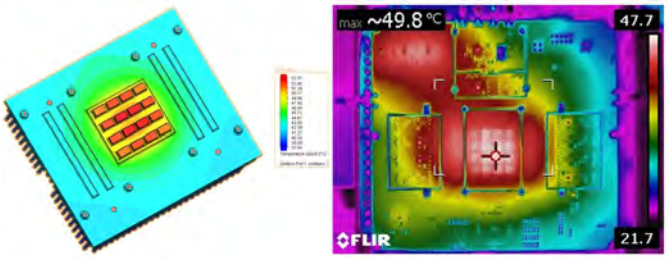

Fig. 19. Thermal model of carrier PCB heat-sink (left) and measured temperature profile of carrier PCB during 256-element continuous transmit operation (right).

has 525 flip-chip pads that are used for power supply, digital I/O, RF, and IF signals and has a total area of $8\times4.4\,\text{mm}^2$. It is important to note that the size of the RFIC can directly impact the antenna spacing in the final system. To be able to maintain a uniform antenna spacing between multiple tiles, the RFIC dimension must be smaller than a single-tile dimension. The die photograph of the chipset is shown in Fig. 13. Each chip operates from 1.5 to 2.5 V. Each power supply within the IC uses a dedicated metal layer to aid in distribution and optimize signal integrity. The transmit/receive phased-array elements consume on average 275/225 mW, while the LO generation block requires 200 mW in the master mode and 75 mW in the slave mode. The baseband and up- and down-converters consume 500 mW in total.

Individual tiles can be self-tested prior to assembly on the final PCB carrier in a low-cost test fixture. This step ensures that only functional tiles are used in the final assembly in order to maximize the system yield. A conventional pogo-pin test socket was designed to be compatible with both 16TX/8RX and 8TX/16RX tile types. The socket is attached to a test

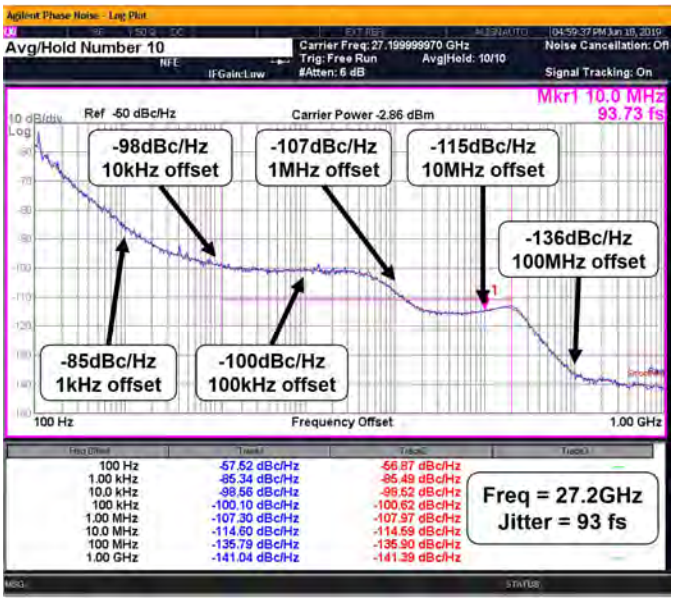

Fig. 20. Measured phase noise performance of the integrated 27-GHz PLL in the master mode which produces the LO synchronization output signal from the first tile. The reference frequency is generated by an external PLL operating at 1.7 GHz.

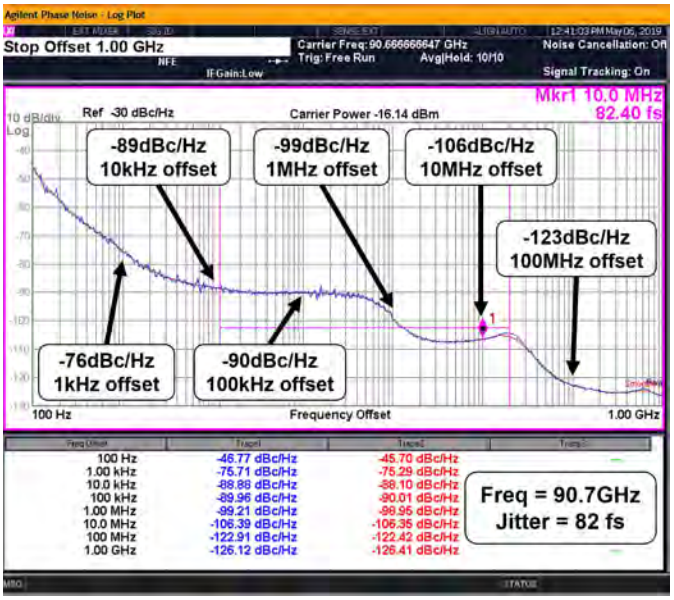

Fig. 21. Measured phase noise of the radiated RF carrier frequency at 90.7 GHz derived from the LO synchronization signal. The reference frequency is generated by an external PLL operating at 1.7 GHz.

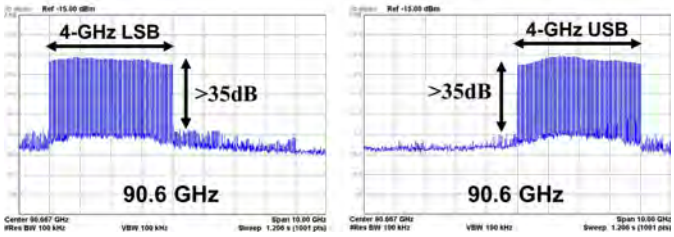

Fig. 22. Measured broadband upper and lower sideband spectrum of the transmitter at a 90.6-GHz carrier. The IF input signal consists of four-hundred 10-MHz-spaced signal tones spanning dc to 4 GHz. An average image rejection of better than 30 dB is observed.

PCB with all the necessary signals for digital interface as well as any instrumentation for further debugging and characterization. The internal diagnostic procedures can measure many of the critical parameters of each tile, while phase-noise, image-rejection, and radiation patterns can be measured using the external measurement equipment. Furthermore, calibration circuitry on the up- and down-convert mixer LO paths provides a mean of further image rejection improvements by the modem through the SPI. The impact of image rejection on constellation error vector magnitude (EVM) is described in [34].

Fig. 8 shows the simplified block diagram as well as specific measurement points for the LO synchronization signal across the multi-tile phased-array system. All integrated jitter measurements span from 12 kHz to 20 MHz, and all phase noise measurements are reported at a 100-kHz offset from the carrier. The external PLL is configured to generate a 1.7-GHz reference signal using a surface-mount 100-MHz VCXO module.

The fundamental PLL output frequency (27 GHz) of the first tile in the chain is measured at the output of the synchronization signal, which is marked as A in Fig. 8. It can be observed that the internal PLL provides an integrated jitter of approximately 90 fs and has a phase noise of 100 dBc/Hz at 100-kHz offset from the carrier (see Fig. 20). Furthermore, it is possible to measure the performance of the internal prime-ratio multiplier using on-chip probing (45-GHz signal marked as B in Fig. 8). The prime-ratio 5/3-multiplier provides the measured rejection of better than 25 dBc for all harmonics ranging from 9 to 69 GHz across the entire locking range of the internal PLL. Furthermore, the measured phase noise at 45 GHz shows that the total integrated jitter remains approximately constant (better than 90 fs), indicating that the prime-ratio multiplier does not degrade the overall phase noise.

The phase noise of the multiplied carrier LO signal can also be measured over the air (marked as C in Fig. 8) using radiated power and is shown in Fig. 21. Similarly, the measured phase noise shows a theoretical increase of 10 dB to −90 dBc/Hz within the PLL bandwidth. Finally, in order to demonstrate that the daisy-chain LO architecture does not adversely impact the phase noise of the LO synchronization signal across the tiles, the phase noise of the synchronization signal from the 16th tile in the chain is also measured (marked as D in Fig. 8). The measured phase noise remains virtually unchanged and is better than 90 fs. All phase noise measurements were performed by using a combination of Rhode & Schwarz FSW85 spectrum analyzer, WR-10 pyramidal horn antenna, Keysight M1970W, and N9030A spectrum analyzer.

A. Phased-Array Transmit and Receive Performance

The measured broadband image rejection of the transmitter at a carrier frequency of 90.7 GHz is shown in Fig. 22. The input baseband signal consists of four-hundred 10-MHz-spaced tones spanning dc to 4 GHz. Depending on the relative phase of the baseband signals, an upper sideband

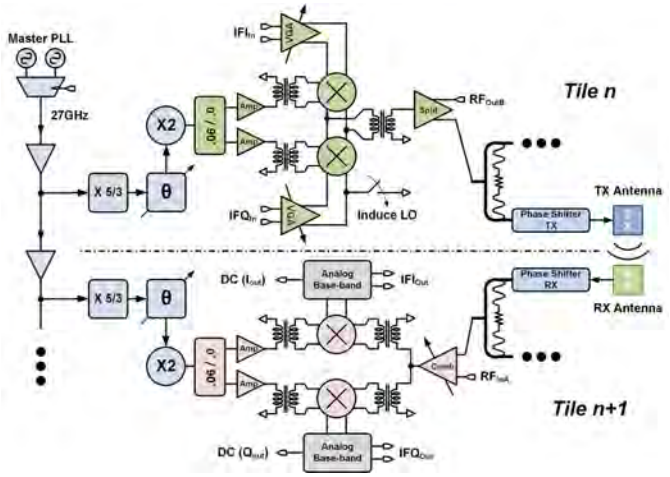

Fig. 23. Block diagram of the tile-to-tile coupling architecture used for system alignment and synchronization.

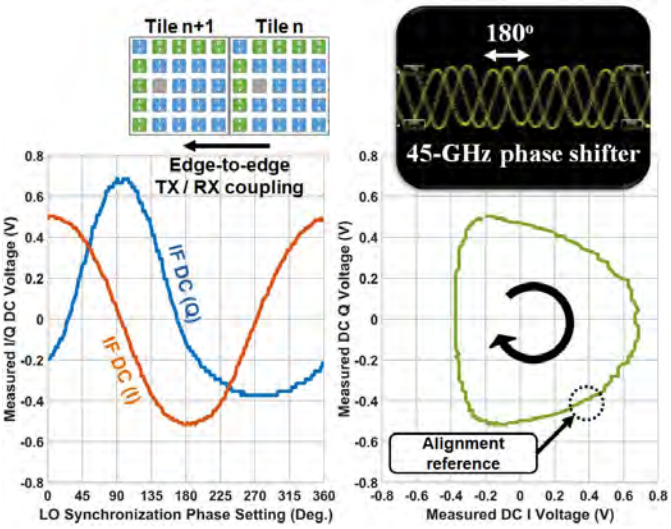

Fig. 24. Measured tile-to-tile coupling phase as a function of the LO phase shifter. An alignment reference point is used to set the LO phase shifter for every coupled tile.

or lower sideband output spectrum is generated. On-chip DACs on all four baseband inputs apply dc offsets to improve carrier suppression. A single setting is maintained for the DACs in this measurement, and the broadband image-rejection and carrier suppression results in better than 35 dB across an 8-GHz output RF spectrum. This improved image rejection result compared with [8] is accomplished through layout optimization of the quadrature hybrid and better matching between the I/Q LO paths in the up-converter mixer block.

1) Multi-Tile Self-Alignment Procedure: The self-alignment procedure utilizes the existing coupling between the adjacent tiles in a large-scale phased-array system to measure the relative LO phase between every neighboring tile. Fig. 23 shows the signal path involved in measuring the relative LO phase between two tiles. The LO signal can be generated by applying a dc offset to the transmit mixer, and the induced dc offset at the receiver is measured at the dc offset cancellation

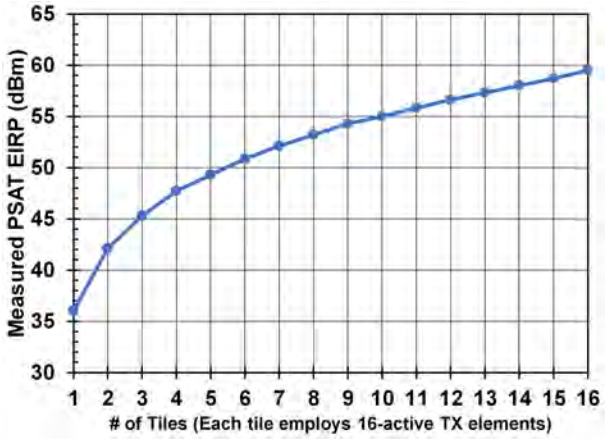

Fig. 25. Measured saturated EIRP at 90.7 GHz as a function of active tiles.

loop of the baseband block. Since the up- and down-conversion mixers use direct-conversion, the measured 0-Hz receiver IF signal corresponds to the relative LO phase between two adjacent tiles. The transmitter LO phase shifter is swept from 0° to 360° and the received I/Q signals are measured internally via on-chip ADCs, as shown in Fig. 24. This process is repeated across all 16 tiles where every LO phase shifter is adjusted until the desired alignment point is reached. Upon the completion of this process at power on, the system is fully aligned. At a sustained SPI rate of 50 MHz, the entire alignment and the calibration process can be completed in less than 10 s.

The measured saturated effective isotropic radiated power (EIRP) of the multi-tile phased array is shown in Fig. 25. A single tile with 16 transmit elements provides a saturated EIRP of approximately 36 dBm. As successive tiles (each containing 16 transmit elements) in the daisy-chained architecture are phase-aligned and enabled, the measured saturated EIRP closely follows the expected $20\log(N)$ power increment, where N is the number of active tiles. With all 16 tiles enabled and 256 transmit elements active, the measured saturated EIRP of the complete phased array is approximately 60 dBm at 90.7 GHz.

The expected performance of the receive phase-shifter elements, including NF and gain, is presented in [8]. In addition, this RFIC generation includes built-in diagnostic tools, which can be used for health monitoring and fault detection. Fig. 26 shows an example diagnostic readout from the 128 receive elements within the full phased-array system. In this particular measurement, the diagnostic tool is configured to measure the received power uniformity, while the biasing in two receiver elements has been purposely disrupted. In a scenario where any failure is detected, the potentially faulty array elements can be disabled in order to avoid radiation pattern or signal degradations.

Since this phased-array system is intended to operate in the TDD mode, the transmit/receive switching time must be minimized. The measured receive-to-transmit switching speed is below 50 ns for all system transmitter gain and beam patterns. The transmit-to-receive switching speed is limited by the settling time of the dc cancellation loop of the analog baseband block. In the worst case scenario, the switching

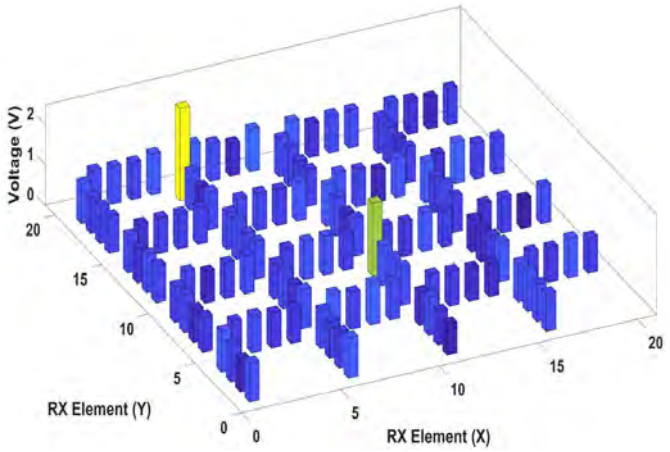

Fig. 26. Instance of measured diagnostic information from 127 receive elements where two elements have been purposely mis-configured to emulate failure.

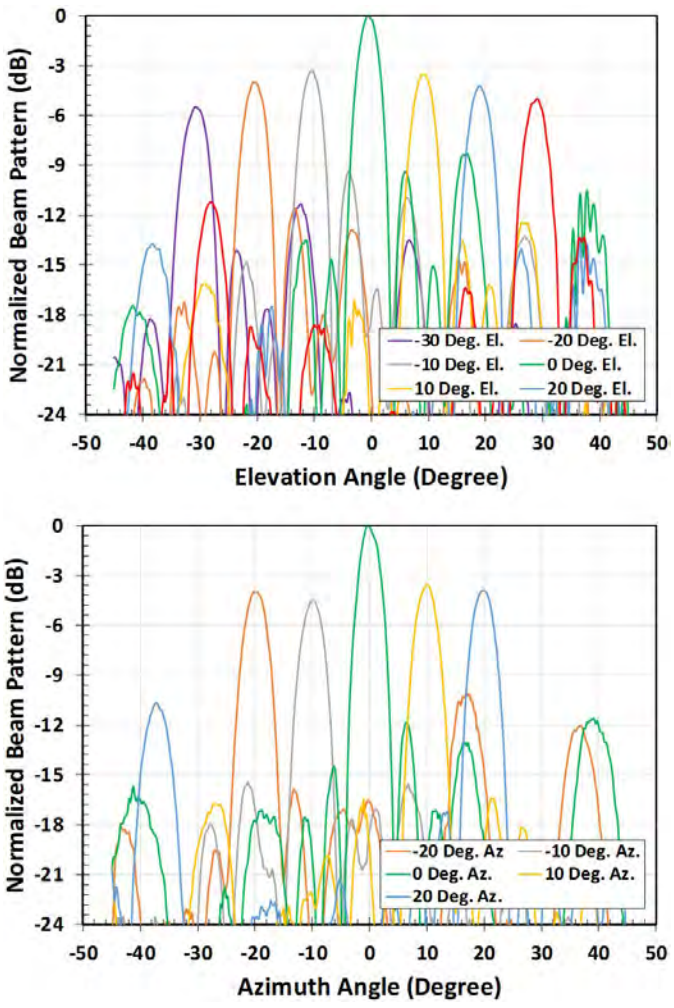

Fig. 27. Measured co-polarization 256-elements, 16-tiles transmit beam patterns in both the E- and H-plane.

speed is below 5 μs. However, depending on the desired modulation format and RF channel bandwidth, the switching speed can be improved by increasing the dc offset cancellation bandwidth.

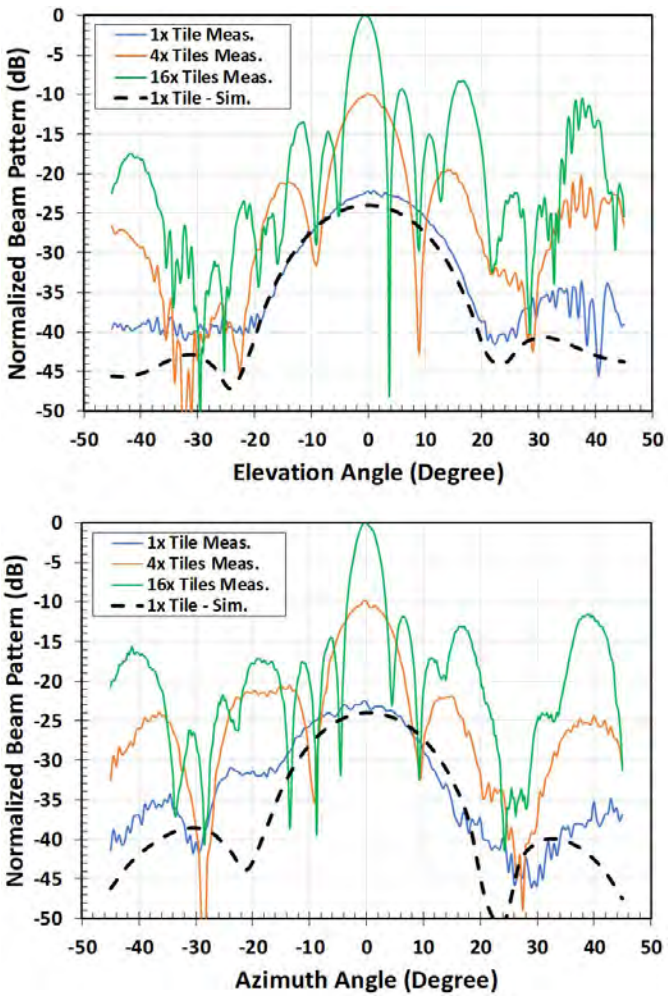

Fig. 28. Measured co-polarization for 16-element, 1-tile, 64-element, 4-tile, and 256-element, 16-tile transmit beam patterns in both the E- and H-plane. The full EM-simulated pattern of a single tile in isolation is also presented.

B. Multi-Tile Beamforming and Beam Hopping Performance

The theoretical maximum scanning angle (with acceptable sidelobe rejection of better than 10 dB) is calculated to be $\pm 36°$ using the following equation:

$$\theta_{\max} = \sin^{-1}\left(\frac{\lambda_{cf}}{d} - 1\right) \tag{1}$$

where λ_{cf} and d represent the 90-GHz center frequency and 0.63λ antenna element spacing in both the E- and H-plane, respectively. It is important to note that 1 assumes a uniform array, while the implemented array is quasi-uniform. However, simulations of the modeled 256-element quasi-uniform array (see Fig. 11) indicates that this approximation is valid to within a few degrees. This is because despite some gaps, the TX array is mostly uniform due to the relatively large number of elements that are spaced at a constant 0.63λ.

Fig. 27 shows the measured E- and H-plane co-polarization beam patterns for 256 transmit elements using 16 active tiles. Phase-shifter settings are programmed into the beam-hopping table in order to steer the beam from $-30°$ to $+30°$ in $10°$ increments. The measured 3-dB beamwidth is

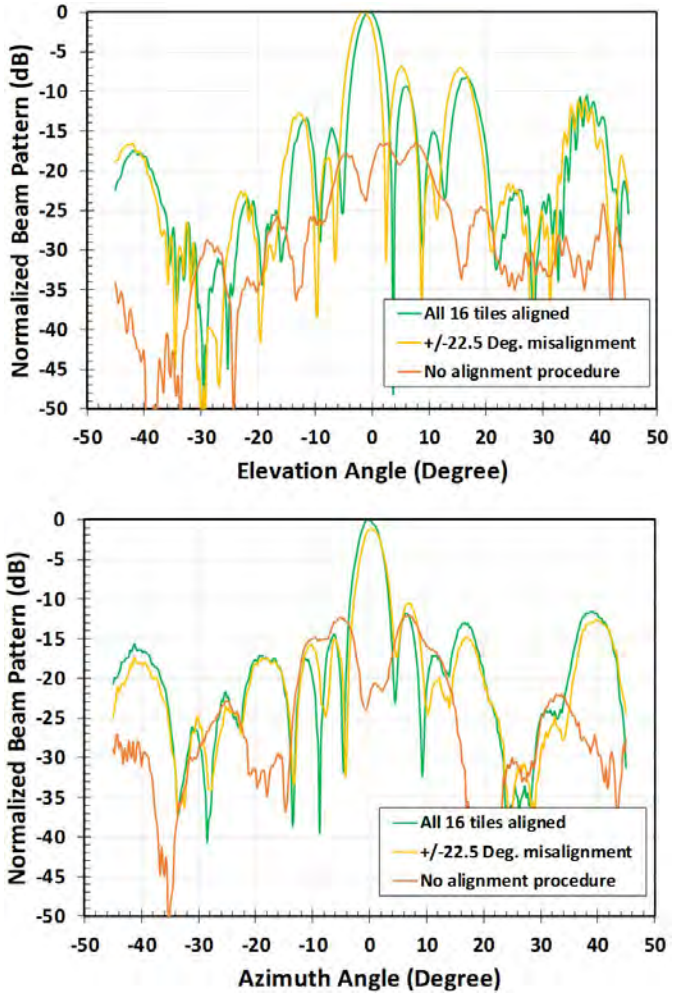

Fig. 29. Measured co-polarization effects of automatic LO alignment procedure on boresight beam pattern in both the E- and H-plane.

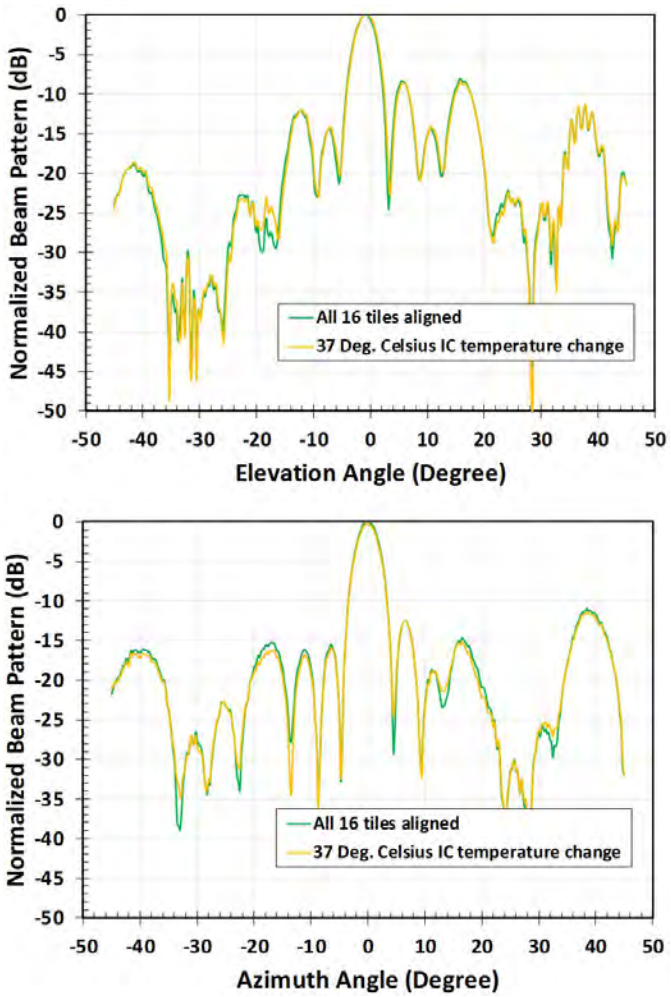

Fig. 30. Measured co-polarization effects of elevated operating temperature on boresight beam pattern in both the E- and H-plane.

approximately 4° for each beam pattern, and sidelobe levels range from −6 to −12 dBc. The only observed grating lobe appears for the +30° beam pattern and is measured at 6 dBc. The asymmetry of the sidelobes is expected due to sub-array asymmetry and sparsity [6], [35]. The measured E-plane co-polarization beam patterns for the 256 transmit elements for beam steering from −20° to +20° in 10° increments behave similarly. The measured 3-dB beamwidth, as expected similar to that in the H-plane due to the uniform spacing, is approximately 4° for each beam pattern with sidelobe levels again ranging from −6 to −12 dBc. It is important to note that aside from tile-to-tile alignment procedure, no other calibration is applied to the phase-shifter elements. Furthermore, all measurements are performed without applying any amplitude tapering to the elements. The measured beam hopping speed for all pre-stored 32 beam configurations and element gains is below 50 ns.

The measured impact on beam pattern in the E- and H-plane based on the number of enabled tiles is presented in Fig. 28. The beam pattern at boresight in both planes becomes increasingly more directive as more phase-aligned tiles are enabled. There is an approximate 12-dB difference in the measured peak transmitted radiated power between 1 tile (16 elements) and 4 tiles (64 elements) as well as between 4 and 16 tiles (256 elements). The measured 3-dB beamwidth for 1 and 4 tile(s) is approximately 16° and 8°, respectively, which is consistent with the expected theoretically calculated values. Furthermore, the EM-simulated radiation pattern of a single tile is also presented. It is important to note that the simulated result does not include the boundary effect introduced by adjacent tiles which is present in all measured results.

Fig. 29 shows the effectiveness of the tile-to-tile phase alignment procedure. With all tiles enabled and no tile-to-tile alignment procedure, the relative phase between every tile is randomized, and therefore, a random beam pattern is observed. However, after the alignment procedure, 20 dB of improvement in the peak transmitter beam at boresight is measured. This comparison demonstrates the importance of the self-alignment procedure during system power-on. Furthermore, by intentionally introducing minor misalignments between [−22.5°, 22.5°] to each tile in the full system, sidelobe levels and peak boresight radiated power remain nearly unaffected. This observation is consistent with the simulated behavior presented in Section II-D and Fig. 12.

TABLE I
COMPARISON OF STATE-OF-THE-ART *W*-BAND PHASED-ARRAY INTEGRATED CIRCUITS

	This Work	[6], [21], [22]	[35]–[37]	[38], [39]	[40]	[41]	[7]
Frequency (GHz)	**80-100**	94	86 – 96	76-84	90-100	108-114	92-98
Elements per RFIC	**16TX/4RX or 8TX/16RX**	16TX/32RX	16TRX/32RX	16RX	16TRX/32RX	16TX	1TRX/2RX
Phased Array Total Elements	**384**	64	64	16	16	16	N/A
Self-test	**Yes**	No	No	Yes	No	No	No
Conversion	**Direct I/Q**	Sliding IF I/Q	Sliding IF I/Q	Direct I/Q	N/A	N/A	N/A
TX P_{SAT} per Element (dBm)	**6 – 8**	>6.5	>2	N/A	-5	1.5	1.4 – 5
Total EIRP (dBm)	**60**	N/A	N/A	27.1	N/A	17 – 24.5	N/A
TX Element DC Power (mW)	**275**	154	116	N/A	275	211	29 – 40
NF (dB)	**6.5 – 8**	<7	8.5	11.4 – 13	8.5 – 11	N/A	8.9 – 9.3
RX Element DC Power (mW)	**225**	90 – 140 (2RX)	160 (2RX)	62.5 – 75	275 (2RX)	N/A	26 – 39 (2RX)
Wireless Data Rate	**>10Gb/s**	N/A	N/A	N/A	N/A	N/A	N/A
RFIC Integration	**Front-end PLL+VCO Baseband Memory**	Front-end PLL+VCO Baseband Memory	Front-end PLL+VCO Baseband Memory	Front-end Baseband	Front-end	Front-end	Front-end
Antenna Integration	**In-package**	In-package	In-package	On-PCB	N/A	On-die	N/A
Array Scaling	**Multi-tile w/ LO distribution**	Super die w/ IF distribution	4-RFIC w/ IF distribution	N/A	RF distribution	RF distribution	N/A
Die Area (mm^2)	**8.1 x 4.5**	13.5 x 11.3	6.6 x 6.7	5.5 x 5.8	6.6 x 5.9	6.6 x 6.0	1.77 x 1.55
Process	**0.18µm SiGe BiCMOS**	0.13µm SiGe BiCMOS	0.13µm SiGe BiCMOS	0.13µm SiGe BiCMOS	0.13µm SiGe BiCMOS	0.18µm SiGe BiCMOS	0.13µm InP HBT

Since the alignment procedure is applied only once during system power-on, it is important to consider the impact of temperature change on tile-to-tile alignment during operation. Fig. 30 shows the effect of operating temperature on the boresight co-polarization beam pattern from a fully aligned 256-element, 16-tile transmitter in the *E*- and *H*-plane. The measured radio-head operating temperature was increased from 50 to 60 °C by purposely throttling the system's cooling fan, which corresponds to beyond 37 °C temperature shift at the IC level. No significant impairment to the beam pattern is observed, while the saturated PSAT of the entire array degrades by approximately 1 dBm.

Due to the system's ability to produce an EIRP of nearly 60 dBm and beam widths of less than 4°, it is possible to visualize the transmitter beam through mm-wave radiation to thermal energy conversion. Using the setup shown in Fig. 32, an RF absorber is placed within the Fresnel zone of the transmitter. By observing the absorber though a Flir IR camera, the beam spot can be viewed thermally as the temperature of the absorber rises up to 15 °C above ambient. Furthermore, combining this method with beam hopping, various letters and shapes can be drawn thermally on the surface of the RF absorber, as shown in Fig. 31.

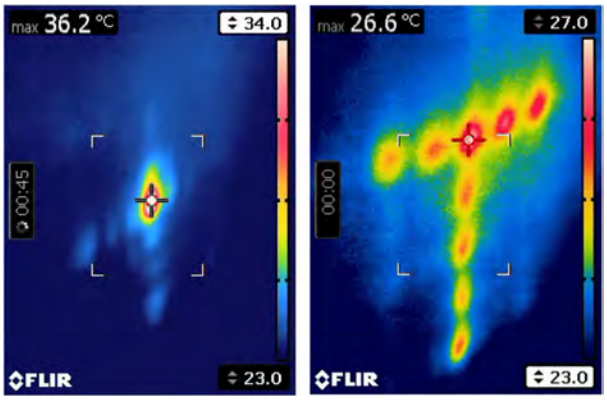

Fig. 31. MM-wave to thermal conversion technique used for beam visualization. IR measurement of 256-element, 16-tile transmitter beam (left), and beam hopping to generate the letter T (right).

C. Wireless Link Measurements

All wireless link measurements are made in a laboratory environment either between the large-scale phased-array system and measurement instruments or a single 8TX/16RX phased-array tile. At 90.7 GHz, the free space path loss at a distance of 5 m is 86 dB using

$$\mathrm{FSPL} = 20\log_{10}(d) + 20\log_{10}(f) + 20\log_{10}(4\pi/c) \qquad (2)$$

where f is the carrier frequency and d is the distance in meters. Fig. 32 shows the measurement setup between the phased-array system and a Keysight M1970W *W*-Band Smart Mixer in conjunction with an N9030A PXA. The phased array is configured at a back-off of 8 dBm from its saturated EIRP in order to produce an EIRP of 52 dBm using a 32-QAM modulation from a Keysight M8190A. The baud rate is limited to 100 MB/s (500 Mb/s using 32-QAM) due to the limited Smart Mixer bandwidth used in measurement. In order to measure the EVM in the absence of the internal PLL phase noise, the 27-GHz LO synchronization signal is provided externally via a Keysight E8257D PSG. The measured EVM using the Keysight 89600 VSA software is below 5%. A wireless link between the transmit and receive phased arrays has also been established with both transmit and receive PLLs active. An additional 35 dB (±0.5 dB) of loss is added to the link by placing an RF absorber in the radiation path. The RF absorber is equivalent to a theoretical link distance in excess of 265 m. Fig. 32 shows the wireless link setup between 256 transmit elements and 16 receive elements. The

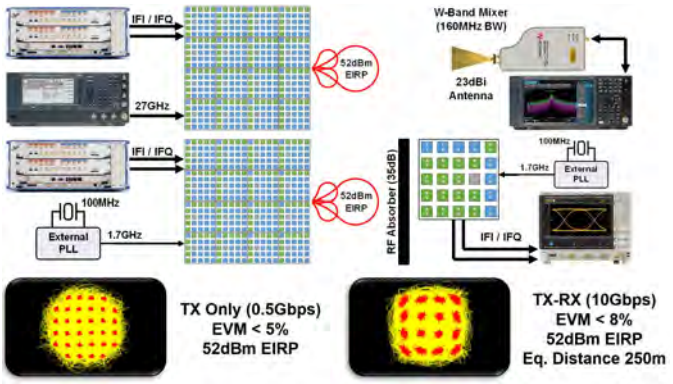

Fig. 32. Top: wireless transmitter measurement setup at 52-dBm EIRP against a reference Keysight mixer. Bottom: wireless link measurement at 52 dBm against a single 16-element receive tile at an equivalent distance of 250 m.

system EVM at 2.5-Gbd (10-Gb/s), 16-QAM constellation is measured using a Keysight MSOS804A oscilloscope to be better than 8%. It is important to note that this measurement includes all system imperfections, including transmit/receive PLL phase noise, non-linearities, I/Q imbalance, bandwidth limitations, and noise. Carrier frequency offsets caused by differences between the crystal oscillators of the two radio heads are compensated for by the modem in the digital domain.

VI. Conclusion

This paper presents a fully integrated phased-array transceiver chipset for steerable-beam and spectrally efficient wireless data links at *W*-Band. By incorporating the RFIC and antennas into a PCB tile, a scalable architecture is presented. The completed system includes a 384 element, 16-tile phased array with built-in self-alignment and self-test utilizing a daisy-chained LO synchronization signal. A maximum saturated EIRP of approximately 60 dBm (1 kW) is achieved at 90.7 GHz by enabling all 256 transmit elements. The daisy-chained LO synchronization signal shows no degradation in phase noise, which offers the possibility of producing large-scale arrays up to thousands of active elements. Further improvements to beam patterns can be made through amplitude tapering across elements or tiles in the current system. However, to produce a uniform array in both the TX and RX apertures, bidirectional TRX elements must be implemented. This can be accomplished at the cost of NF and linearity, which allows the designers to trade off various system requirements. Wireless system measurements are consistent with theoretical prediction of beam pattern behavior as a function of tile-to-tile alignment and calibration. This system is well suited for a range of applications, such as ultrahigh-capacity PTP and PTMP backhaul. Table I shows the comparison of state-of-the-art mm-wave phased arrays up to and including *W*-band frequency range [35]–[41].

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