Summary of SMTA
Important Testability Guidelines

Probe and Fixture Guidelines

1. Test Pads/Vias on all Nets.
2. Index Tolerance + 0.002 inches Datum to Test Pad.
3. Two Tooling Holes on UUT + 0.002 Tolerance between them.
4. Tooling Hole Diameters + 0.0031 / -0.000 inches.
5. Test Pad / Via Pad Size 0.035 to 0.040 inches.
6. Test Pad / Via Pad Separation 0.015 inches.
7. Test Pad Center to Center Spacing.

Priority	Preferred	Acceptable
1	0.100”	0.085”
2	0.075”	0.070”
3	0.050”	0.050”

8. Locate all Test Pads on one side of board if possible.
9. Keep Component Height on probe side less than 0.255 inches.
10. No components or test pads closer than 0.125” from edge of UUT.
11. No resist on test pads.
12. Fill through hole vias with solder
13. No probing of component leads.
14. Distribute test pads evenly over PC Board.
15. Provide clearance space for fixture push finger.
16. Minimize fixture changes when redesigning boards

Other, important SMTA Board Layout Guidelines are given for:

a. Vectorless Test
b. Automated Optical Inspection
c. X-Ray Inspection

Electrical Design Guidelines

1. Provide Test Access to All Electrical Nodes.
2. Place Test Pads as close as possible to signal source.
3. Include 2 Test Pads on each Electrical Node tied to Critical Low Impedance.
4. DO NOT rely on edge connector, circuit traces, or SMT Device Pads for Test Points.
5. Use pull up and fill down resistors for control of IC Control Lines.
6. Include Test Pads for unused Device Pins.
7. Includes method to disable Clock Sources.
8. Provide Disable methods for ALL Programmable Logic Devices.
9. Include Pull-up loads on all open device inputs.
10. Provide disable methods for all Bussed Devices, High Current Devices, and Devices tied to Flash, Rams, EEProms, and D/A Converter.
11. Include – circuitry to Disable Feedback Loops.
12. Use Devices with short Initialization Times.
13. Provide Vectors for all ASIC and Custom Devices
14. In using Vectorless test don't use devices with heat sink or ground plans on top.
15. Supply Documentation for Device Logic Function.
16. Use IEEE 1149 Boundary Scan and 1149.4 Analog and Mixed Signal compatible devices.
17. Isolate Power – On Reset Circuits from other digital devices.
18. Place Test Pads and Power and Ground Nodes as close as possible to each Digital Devices under test.
19. Use multiple test pads on power and ground connections.
20. Allow for Battery Isolation during In-Circuit Test.
21. Buffer Test Pads to Analog and Mixed Signal Devices.
22. Keep In-Circuit Testing in mind when implementing Engineering Changes.
23. See SMTA Electrical Guidelines for more detailed information on the previous topics and if you are combing X-Ray and In-Circuit Test.

Boundary Scan Guidelines

1. Device Selection is critical. Be sure Boundary Scan is truly implemented on the device under consideration.
2. BSDL files are needed for the generation of tests.
3. Verify that the board design complies with BSDL requirements.
4. Test Pads are still needed for all nets on a board.

There are many important Boundary Scan Board Design Rules and recommendations for utilizing the power of Boundary Scan Test and In-System Programming, along with Analog and Mixed Signal Device Testing.

Testing with Built-In Self Test is another very important area with its own guidelines as put forth in the SMTA Testability Guidelines Documentation.